REMARKS

Applicants appreciate the Examiner's thorough examination of the present application as evidenced by the Office Action of July 18, 2005 (hereinafter "Office Action"). Applicants especially appreciate the indication that Claims 5, 6, 11, 19, 23, 26, and 30 recite patentable subject matter and the allowance of Claims 34, 35, and 37. In response, Applicants have amended Claims 5, 6, 8, 12, 19, and 23 to correct various antecedent basis errors to ensure that the Claims satisfy the requirements of 35 U.S.C. §112. Applicants respectfully submit that the cited references do not disclose or suggest, at least, the recitations of the pending independent claims. Accordingly, Applicants submit that all pending claims are in condition for allowance. Favorable reconsideration of all pending claims is respectfully requested for at least the reasons discussed hereafter.

The 35 U.S.C. §112 Rejections

Various claims stand rejected under 35 U.S.C. §112, second paragraph as being indefinite due to antecedent basis errors. In response, Applicants have amended Claims 5, 6, 8, 12, 19, and 23 to correct the antecedent basis errors to ensure that all pending claims satisfy the requirements of 35 U.S.C. §112.

Independent Claims 1, 14, and 43 are Patentable

Independent Claims 1 and 14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U. S. Patent No. 6,438,670 to McClannahan (hereinafter "McClannahan") in view of U. S. Patent No. 6,418,495 to Ryan (hereinafter "Ryan"). Independent Claims 14 and 43 stand rejected under 35 U.S.C. §102(e) as being anticipated by McClannahan. Independent Claim 1 is directed to a memory device controlled by a memory controller and recites, in part:

> ...
> a delay control register for receiving delay control information from the memory controller and storing the received delay control information; and
> ...

Thus, according to independent Claim 1, delay control information is received from the memory controller and stored in a delay control register at the memory device. Claims 14 and

43 include similar recitations. For example, Claim 14 includes the recitation:

> receiving delay control information from the memory controller and storing the received delay control information;

Claim 43 includes the recitation:

> receiving delay control information from the memory controller at the memory device;

Applicants respectfully submit that McClannahan does not disclose or suggest receiving delay control information from a memory controller at another device as recited in Claims 1, 14, and 43. In fact, the Office Action acknowledges that "McClannahan does not explicitly disclose a delay control register for receiving delay control information from the memory controller." (Office Action, page 3). The Office Action alleges, however, that the command/address buffer register 131 of FIG. 1 of Ryan provides the missing teaching. (Office Action, pages 3 and 4). Applicants respectfully disagree with this interpretation of Ryan of FIG. 1 of Ryan. Ryan is directed to a pipelined memory system (Abstract) that incorporates DRAMs 131.* as shown in FIG. 1. Because of the pipeline architecture, a two clock cycle delay is introduced to access the DRAMs. Ryan explains how the design shown in FIG. 1 accommodates this delay as follows:

> Pipelined memory systems 130, however, add a two clock cycle delay to DRAM access. In order to ensure efficient operation, **the packet protocol used for communication is defined to incorporate a first delay for C/A buffer register 131 and a second delay for data register 141.** Furthermore, memory controller 105 issues command and address packets and data packets in pipeline fashion such that the first delay and the second delay do not have a substantial impact on the performance of memory system 100. (Ryan, col. 5, lines 53 - 63; emphasis added).

Thus, in sharp contrast to the recitations of Claims 1, 14, and 43, delay control information is not received at the C/A buffer register 131 shown in FIG. 1 of Ryan. Instead, the packet protocol used by the memory controller 105 and the memory subsystems 130.* is designed to incorporate the appropriate delays when sending command, address, and/or data packets to the C/A buffer register 131. The information actually received at the C/A buffer register is, therefore, command, address, and/or data packets rather than delay control information.

According to Ryan, delay control is built into the communication protocol.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claims 1, 14, and 43 are patentable over McClannahan and Ryan, either alone or in combination, and that Claims 2 - 13, 15, and 44 are patentable at least per the patentability of independent Claims 1, 14, and 43.

Independent Claims 3, 8, 16, 20, and 24 are Patentable

Independent Claims 3, 8, 16, and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over McClannahan in view of to Ryan. Independent Claim 24 stands rejected 35 U.S.C. §102(e) as being as anticipated by McClannahan. Independent Claim 3 is directed to a memory controller for controlling memory modules and recites, in part:

> ...
> a delay control register for receiving delay control information according to a specification from serial presence detectors (SPD) loaded into the memory modules and storing the received delay control information; and
> ...

Thus, according to independent Claim 3, the memory controller comprises a delay control register that receives delay control information from one or more memory modules. The delay control information is stored in SPDs that are loaded into the memory modules. Claims 8, 16, 20, and 24 include similar recitations. For example, independent Claim 24 recites, in part:

> a plurality of memory modules, a respective one of which being responsive to a control signal and having delay control information stored thereon; and
> ...

Thus, according to independent Claim 24, delay control information is stored on one or more of the plurality of memory modules.

The Office Action acknowledges that McClannahan does not disclose a delay control register for receiving delay control information according to a specification from serial presence detectors (SPD) loaded into the memory modules. (Office Action, page 5). The Office Action alleges, however, that the memory system shown in FIG. 1 of Ryan provides

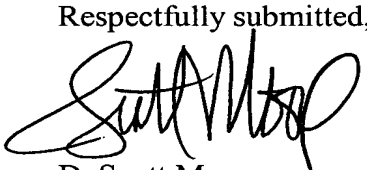
the missing teaching. (Office Action, page 5). Applicants respectfully disagree with this interpretation of the memory system shown in FIG. 1 of Ryan. As discussed above, the C/A buffer register 131 and the data register 141, which are included on each memory subsystem 130.*, do not contain any delay control information thereon. Instead, the packet protocol used by the memory controller 105 and the memory subsystems 130.* is designed to incorporate the appropriate delays when sending command, address, and/or data packets to the C/A buffer register 131. Thus, in sharp contrast to the recitations of Claims 3, 8, 16, 20, and 24, delay control information is not stored on the memory subsystems 130.* of Ryan. As a result, the controller 105 does not receive delay control information from the memory subsystems 130.* nor does the controller 105 generate a control signal responsive to delay control information stored on the memory subsystems 130.*.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claims 3, 8, 16, 20, and 24 are patentable over McClannahan and Ryan, either alone or in combination, and that Claims 4 - 7, 9 - 13, 17 - 19, 21 - 23, and 25 - 30 are patentable at least per the patentability of independent Claims 3, 8, 16, 20, and 24.

CONCLUSION

In light of the above amendments and remarks, Applicants respectfully submit that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,

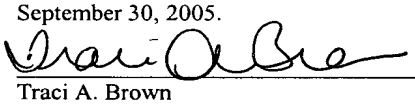


D. Scott Moore
Registration No. 42,011

Customer No. 20792
Myers Bigel Sibley & Sajovec
P. O. Box 37428
Raleigh, North Carolina 27627
Telephone: (919) 854-1400
Facsimile: (919) 854-1401

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on September 30, 2005.



Traci A. Brown